FIG.1

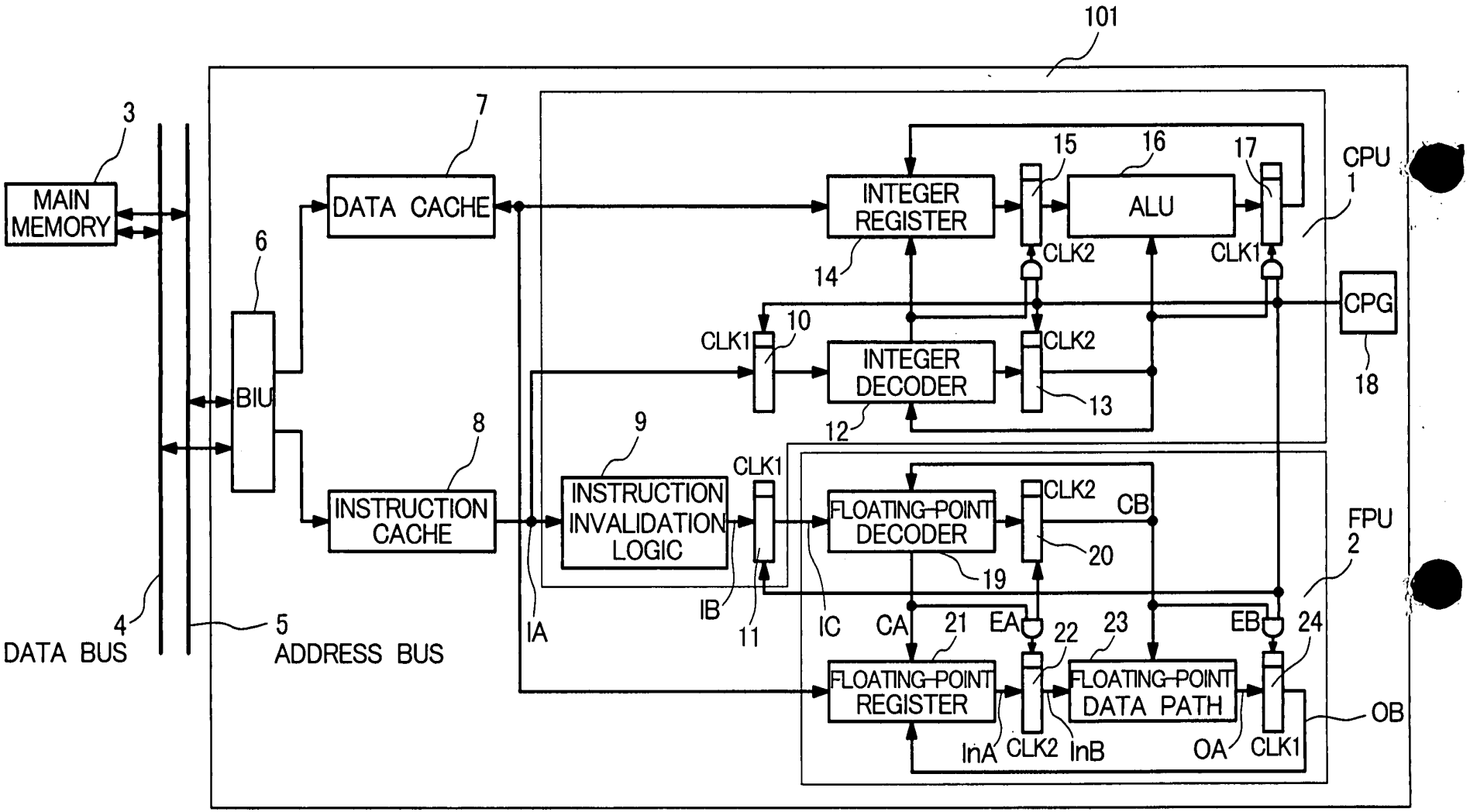

101
3
MAIN MEMORY
7
DATA CACHE
6
BIU
8
INSTRUCTION CACHE
9
INSTRUCTION INVALIDATION LOGIC
CLK1
11
IA
IB
IC
4
DATA BUS
5
ADDRESS BUS
INTEGER REGISTER
15
16
17
ALU
CLK2
CLK1
14
CPU
1
CPG
18
10
INTEGER DECODER
13
12
FLOATING-POINT DECODER
CB
20
19
FPU
2
CA
21
EA
22
23
EB
24
FLOATING-POINT REGISTER
FLOATING-POINT DATA PATH
OB
InA
InB
OA

FIG.2

```
1 FADD  FR0 , FR1  ; FPU INSTRUCTION  1
2  ADD  R0 , R1    ; CPU INSTRUCTION  1
3  SUB  R2 , R3    ; CPU INSTRUCTION  2
4 FDIV  FR2 , FR3  ; FPU INSTRUCTION  2
5 SHAD  R4 , R5    ; CPU INSTRUCTION  3
6  OR   R6 , R7    ; CPU INSTRUCTION  4
```

FIG.3

```
1 FADD  FR0 , FR1  ; FPU INSTRUCTION  1
2  NOP             ; CPU INSTRUCTION  1
3  NOP             ; CPU INSTRUCTION  2
4 FDIV  FR2 , FR3  ; FPU INSTRUCTION  2
5  NOP             ; CPU INSTRUCTION  3
6  NOP             ; CPU INSTRUCTION  4
```

FIG.4

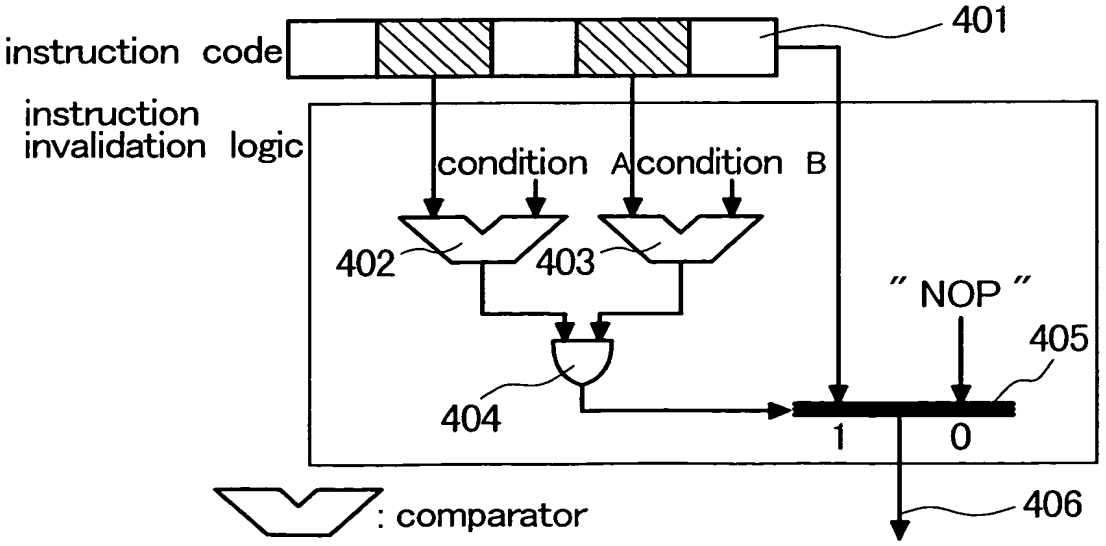


FIG.5

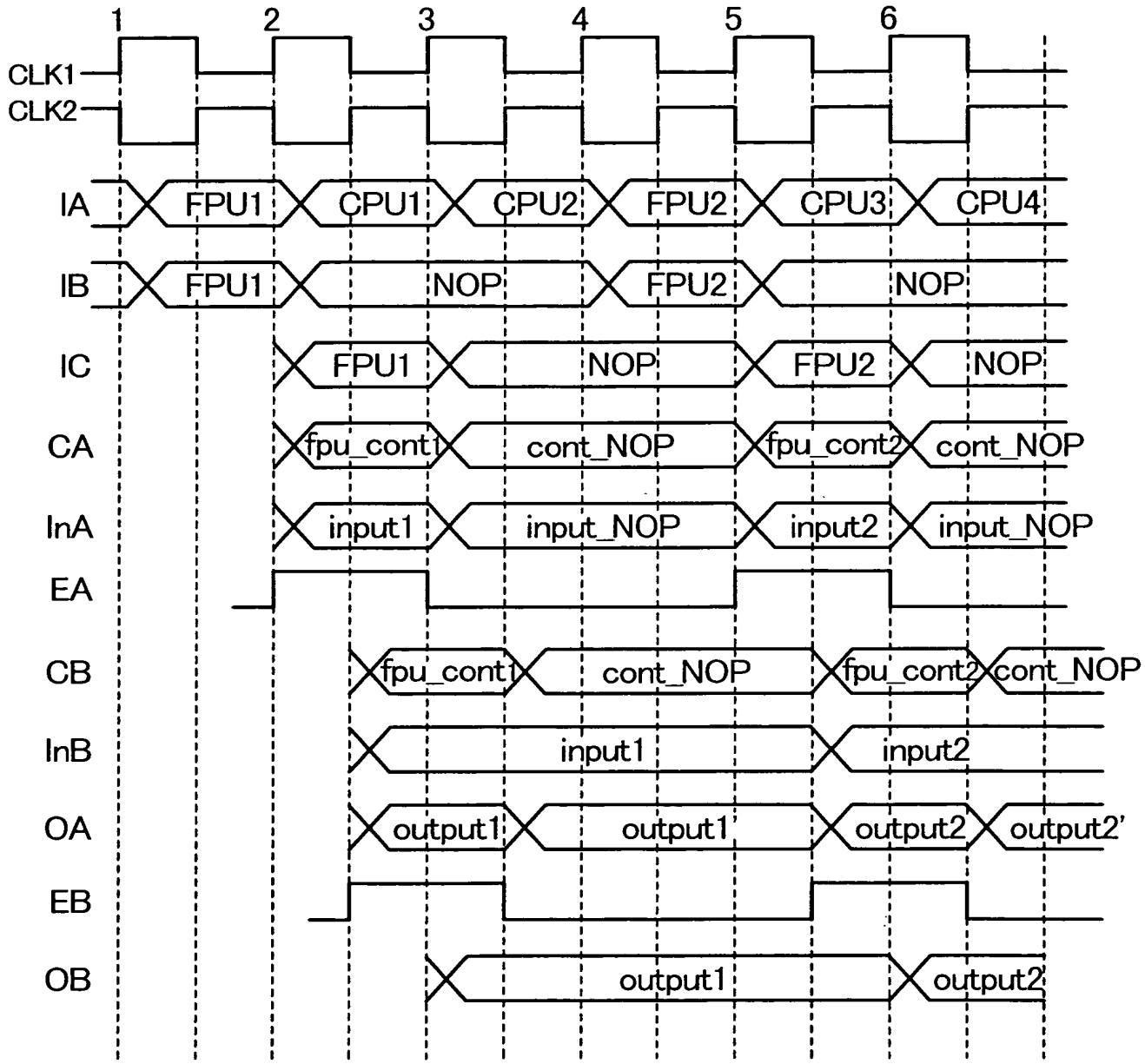

1
2
3
4
5
6
CLK1
CLK2
IA
FPU1
CPU1
CPU2
FPU2
CPU3
CPU4
IB
FPU1
NOP
FPU2
NOP
IC
FPU1
NOP
FPU2
NOP
CA
fpu_cont1
cont_NOP
fpu_cont2
cont_NOP
InA
input1
input_NOP
input2
input_NOP
EA
CB
fpu_cont1
cont_NOP
fpu_cont2
cont_NOP
InB
input1
input2
OA
output1
output1'
output2
output2'
EB
OB
output1
output2

FIG.6

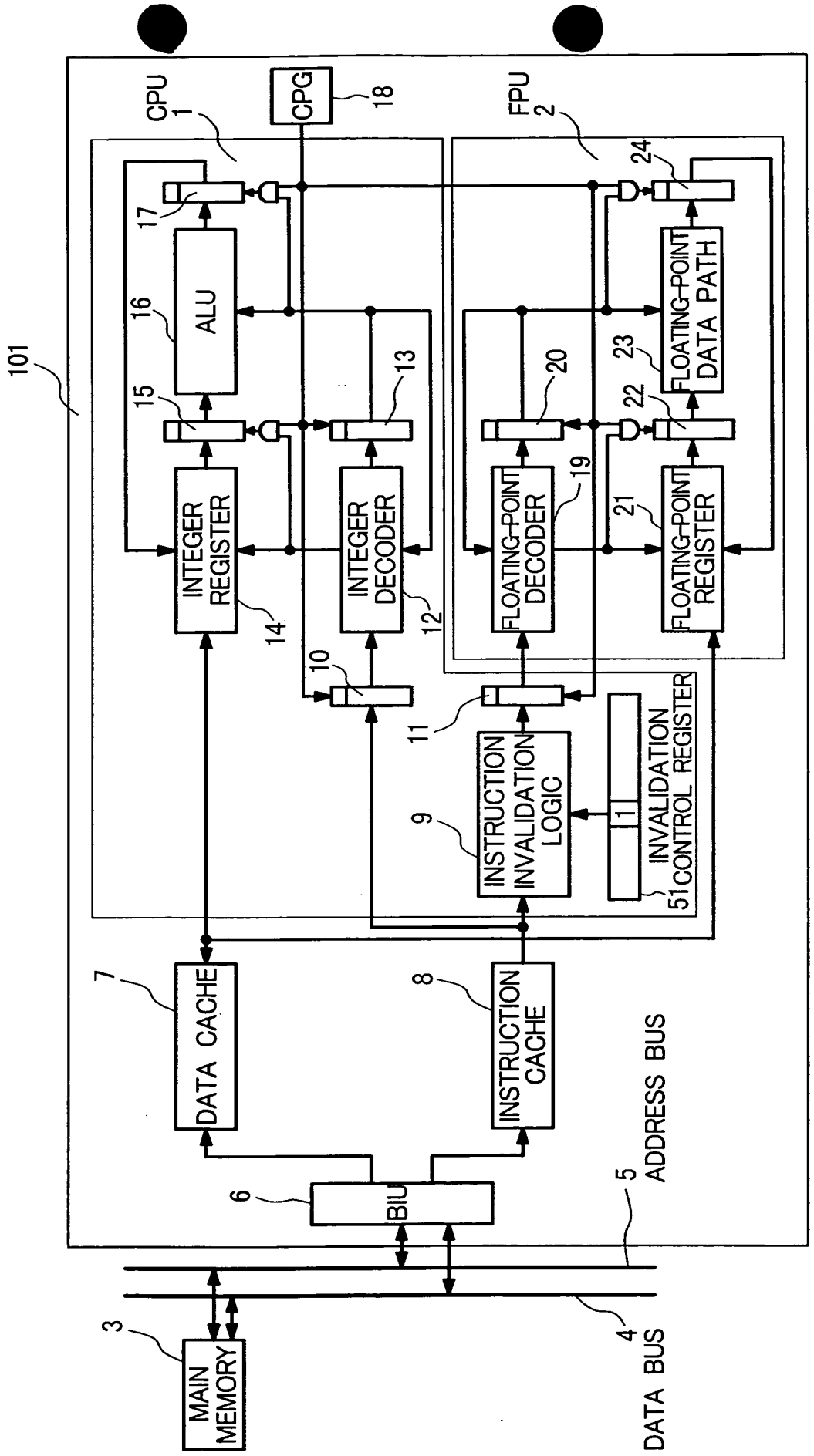

101
CPU
1
CPG
18
FPU
2
17
16
ALU
15
13
INTEGER REGISTER
14
INTEGER DECODER
12
10
11
20
FLOATING-POINT DECODER
19
24
23
FLOATING-POINT DATA PATH
22
21
FLOATING-POINT REGISTER
INSTRUCTION INVALIDATION LOGIC
9
1
INVALIDATION CONTROL REGISTER
51
7
DATA CACHE
8
INSTRUCTION CACHE
6
BIU
5
ADDRESS BUS
3
MAIN MEMORY
4
DATA BUS

FIG.7

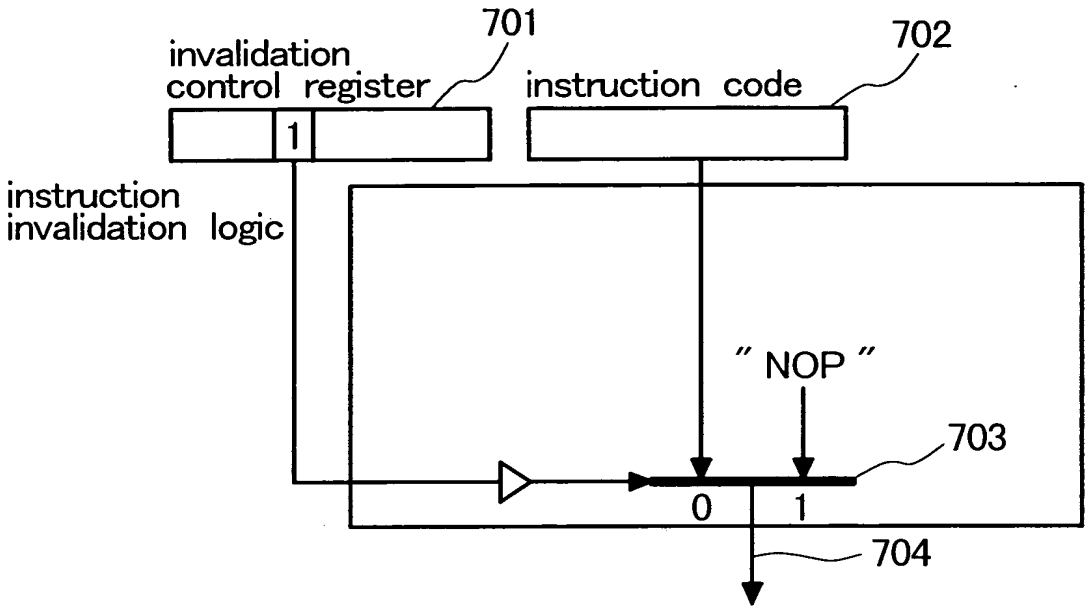

701
invalidation
control register
1
702
instruction code
instruction
invalidation logic
" NOP "
703
0
1
704

FIG.8

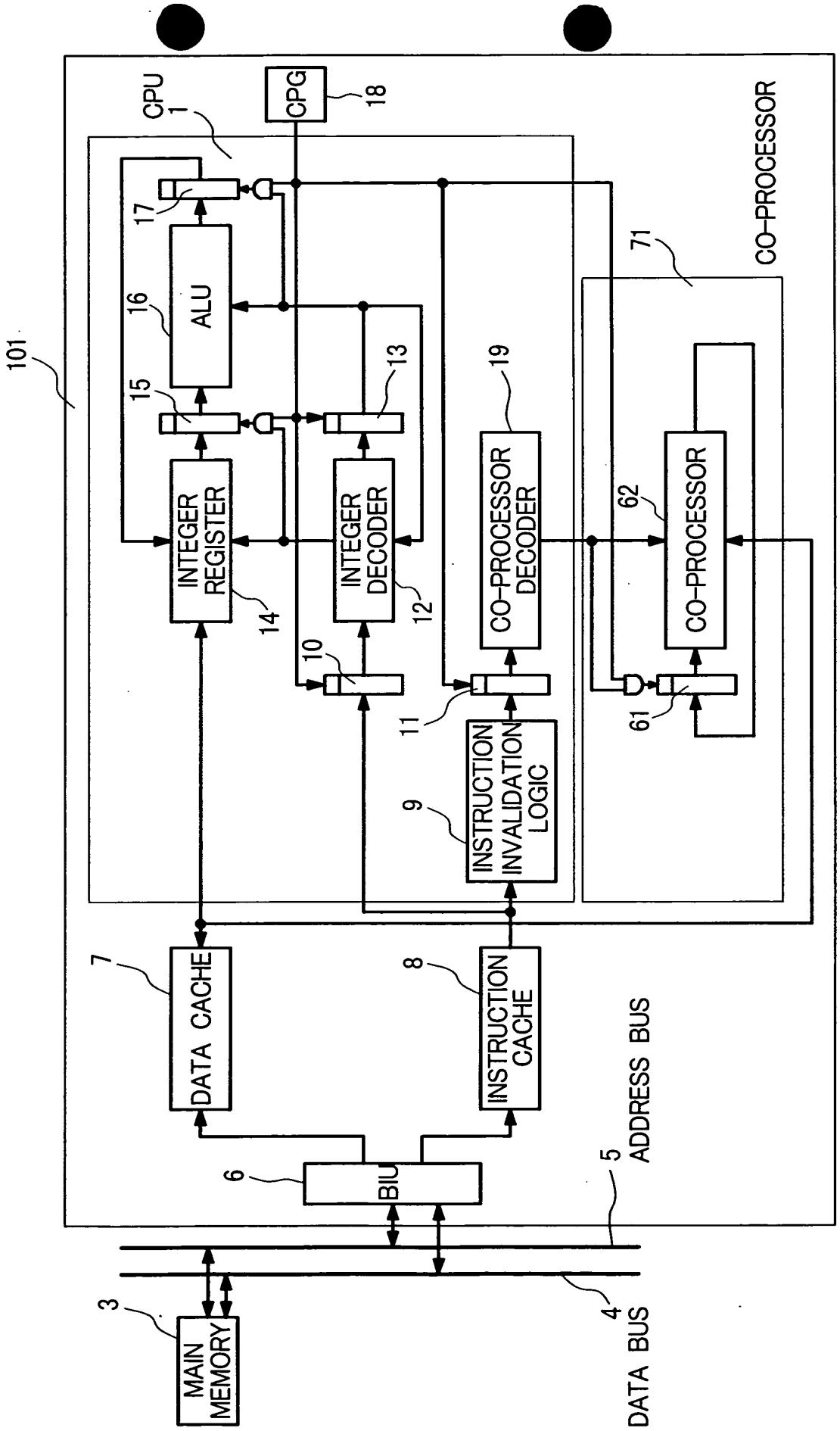

101
CPU
1
CPG
18
17
ALU
16
15
13
INTEGER REGISTER
14
INTEGER DECODER
12
10
11
19
CO-PROCESSOR DECODER
INSTRUCTION INVALIDATION LOGIC
9
71
CO-PROCESSOR
62
61
CO-PROCESSOR
7
DATA CACHE
8
INSTRUCTION CACHE
6
BIU
5
ADDRESS BUS
3
MAIN MEMORY
4
DATA BUS

FIG.9

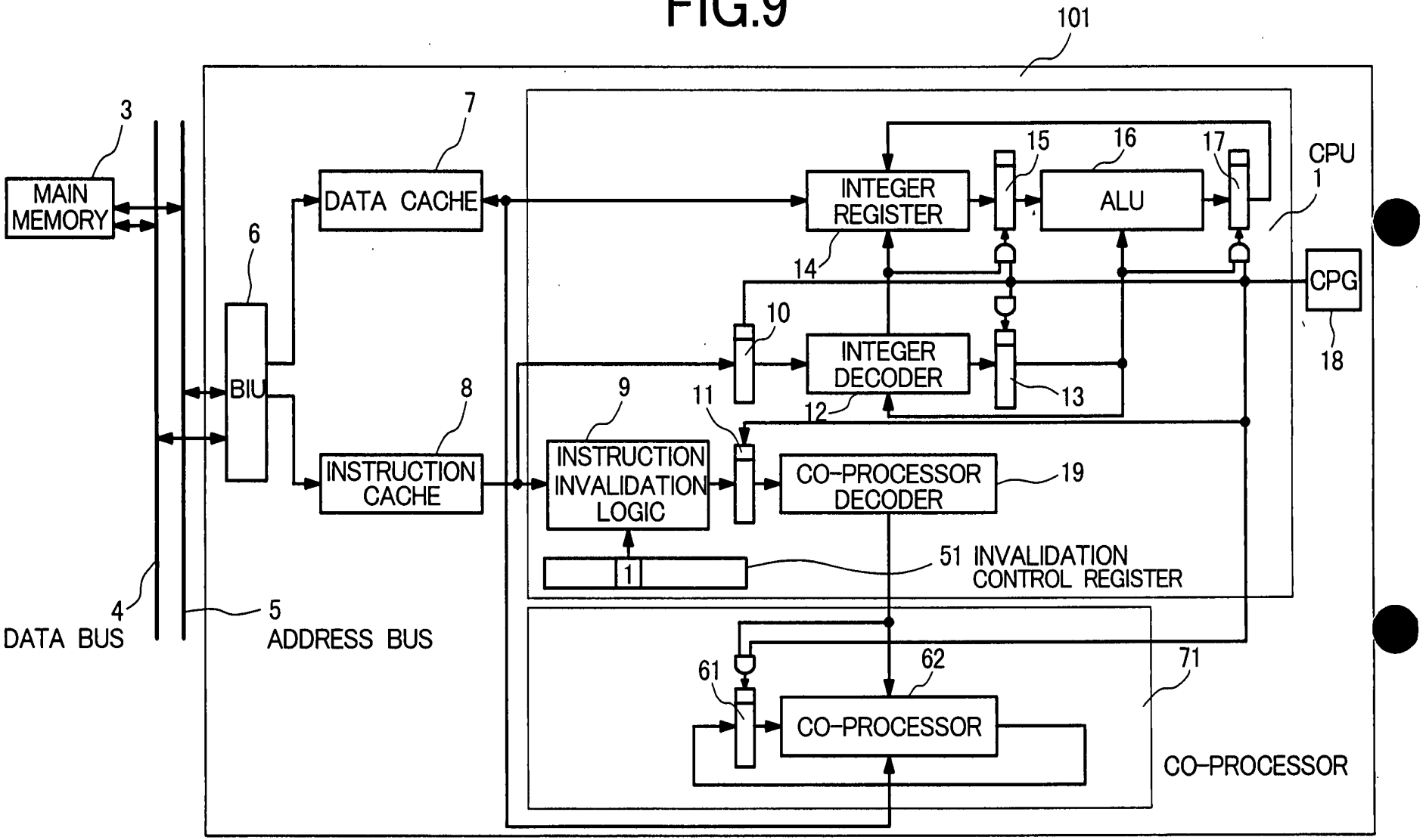
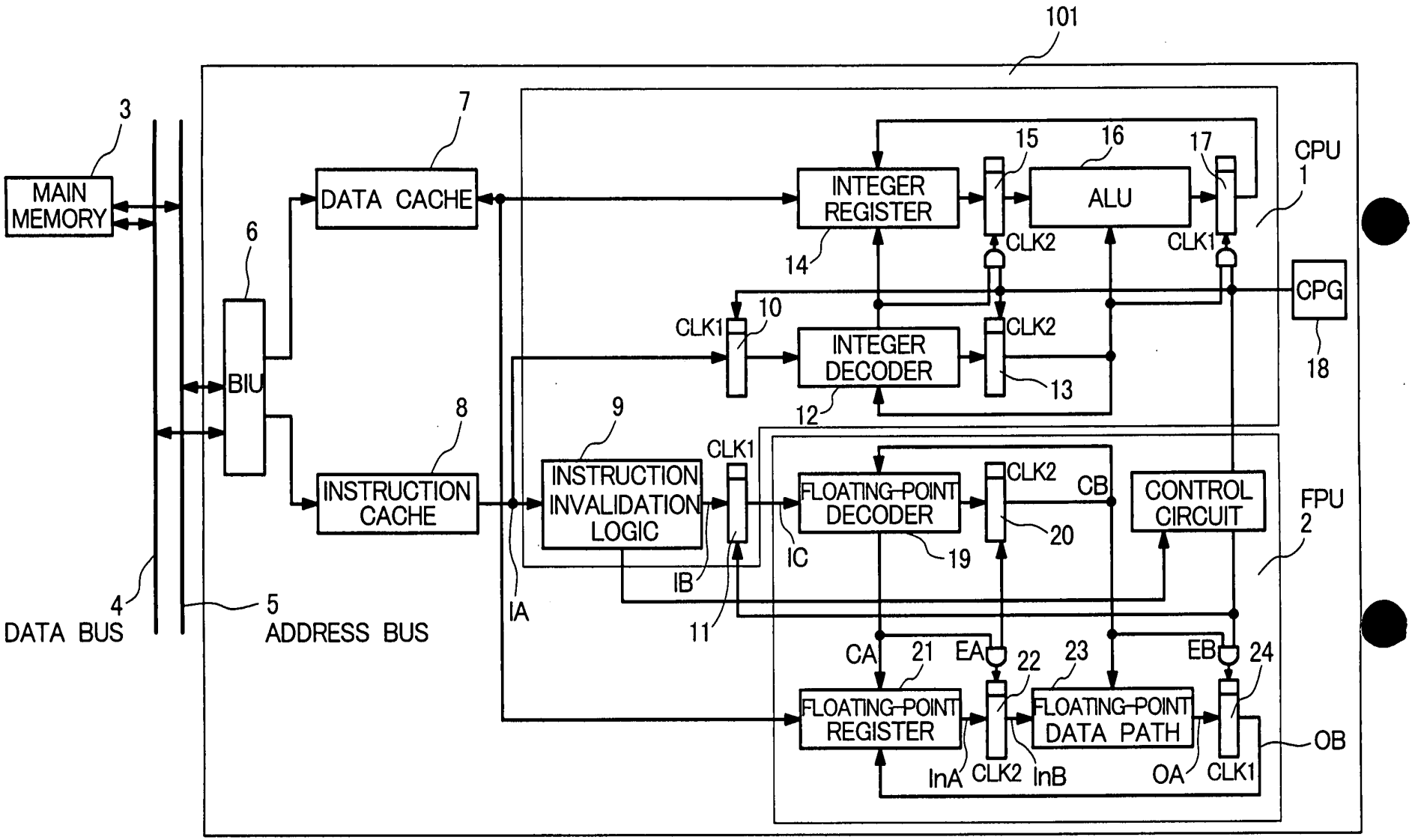

101
3
MAIN MEMORY
7
DATA CACHE
15
16
17
CPU
1
INTEGER REGISTER
ALU
6
14
CPG
10
18
INTEGER DECODER
BIU
8
9
11
13
12
INSTRUCTION CACHE
INSTRUCTION INVALIDATION LOGIC
CO-PROCESSOR DECODER
19
1
51 INVALIDATION CONTROL REGISTER
4
DATA BUS
5
ADDRESS BUS
61
62
71
CO-PROCESSOR
CO-PROCESSOR

FIG.10


101
3
MAIN MEMORY
7
DATA CACHE
6
BIU
8
INSTRUCTION CACHE
9
INSTRUCTION INVALIDATION LOGIC
IA
IB
IC
11
4
DATA BUS
5
ADDRESS BUS
INTEGER REGISTER
14
15
16
17
ALU
CLK2
CLK1
CPU
1
CPG
18
10
INTEGER DECODER
12
13
FLOATING-POINT DECODER
19
20
CB
CONTROL CIRCUIT
FPU
2
CA
21
EA
22
23
EB
24
FLOATING-POINT REGISTER
FLOATING-POINT DATA PATH
InA
InB
OA
OB